REMARKS

Applicants appreciate the thorough examination of the present application that is reflected in the Official Action of October 20, 2004. In response, many of the claims have been canceled, and the remaining independent claims have been amended as will be described below, to place the application in condition for allowance. Applicants respectfully request reconsideration of the outstanding rejections and allowance of the pending claims for the reasons that now will be described.

The Rejections Under 35 USC §112 Have Been Overcome

Claims 1-7 have been canceled to expedite allowance, so that the rejections under 35 USC §112, first paragraph are now moot. Applicants have realized that these claims are unnecessary in view of the breadth of the remaining independent claims, and have canceled these claims to eliminate any issues under 35 USC §112. However, Applicants wish to explain that the periphery of the array is shown, for example, by the Xs in Figure 4 and that, under this definition of "periphery", the recitations of Claims 1 and 7 are entirely consistent with the specification.

The Pending Claims Are Patentable Over Iwasaki '890, Iwasaki '882 and/or Dockerty et al.

In order to place the present application in condition for allowance, the recitations of Claim 11 have been incorporated into independent Claim 8, the recitations of Claim 17 have been incorporated into independent Claim 14, and the recitations of Claim 23 have been incorporated into independent Claim 20. Moreover, Claims 8, 14 and 20 have also been amended to recite:

> a plurality of signal conductors that extend from outside the array of external connectors, along the routing channel, and electrically connect to a plurality of the external connectors in an interior row or interior column adjacent the routing channel.

Support for these amendments may be found, for example, in Figure 3 of the present application and in the accompanying description of the specification.

Original Claims 11 and 23 were rejected under 35 USC §103(a) over Iwasaki '890 in view of Iwasaki '882. The Official Action concedes at Page 7, lines 2-3 that Iwasaki '890 does not describe or suggest the claimed signal conductors, and cites

Iwasaki '882 in an attempt to supply the missing teachings. However, Iwasaki '882 does not describe the above-quoted recitations of Claims 8, 14 or 20. In particular, Iwasaki '882 describes the use of circuit wires **6b** to route peripheral connection pads **6a** to interior via holes **7**, and thereby provide a uniform connection array for a chip that only includes edge pads. For example, as noted in Iwasaki '882 Column 3, lines 13-36:

> The boards, for instance, as shown in the plan view of the form of a main surface of board **6** in FIG. 2, are provided with connection pads ***6a*** adapted to the input/output terminals of the semiconductor chip to be mounted. There is also circuit wires ***6b***, one end of each such circuit wire ***6b*** being electrically connected to one of said connection pads ***6a***; the other end of each wiring circuit ***6b*** is a connection end connected to the back side (other main surface) of the circuit board **6** through a filled via hole (filled via hole connection) **7** installed right above the flat external connector terminals brought out and laid out preferably in a constant-pitch lattice-array. FIG. 3 is a plan view of the form of the back side of the board **6** wherein only external connector terminals **8** are brought out and laid out in a constant-pitch lattice-array. Here, the arrangement of flat external connector terminals **8** leading to and are exposed on the back side of the board **6** is not particularly limited; however, when arranged in said constant-pitch lattice-array, this type of semiconductor package can be standardized. Further, when the arrangement of said external connector terminals **8** is unbalanced, by installing dummy connector terminals **8'** on a corner as shown in FIG. 4, planar installation of semiconductor packages will be easier to perform. (Emphasis added.)

Thus, Iwasaki '882 provides a board that can route an edge-connected chip to an array connected board, as shown more explicitly in Figures 5-6 of Iwasaki '882. However, Iwasaki '882 does not include any discussion of the need to route signal conductors from outside an array of external connectors to interior connectors in the array.

Iwasaki '882 also does not suggest the claimed solution:

> a plurality of signal conductors that extend from outside the array of external connectors, along the routing channel, and electrically connect to a plurality of the external connectors in an interior row or interior column adjacent the routing channel.

As noted in the present application, for example at Page 6, lines 26-28:

> Accordingly, by configuring a routing channel according to embodiments of the present invention, additional access to the interior of the grid array may be provided for routing.

For at least these reasons, independent Claims 8, 14 and 20, and the dependent claims that depend therefrom, are unobvious over the Iwasaki references.

Moreover, Claim 20 is independently patentable because Claim 20 recites:

> ...wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are operationally disconnected from the substrate to define a routing channel that extends from the periphery of the array towards the interior of the array....

The Official Action cites, at Page 6, Iwasaki '890 Figures 8 and 10, and Column 7, lines 30-58, as reciting "dummy/operationally disconnected connectors". However, this passage of Iwasaki '890 clearly notes that these "dummy" connectors are provided outside the array of connectors. See, Iwasaki '890 Column 7, lines 30-58:

> In FIGS. **8**, **9**, and **10**, the external connecting terminals are formed at the center portion of the board and dummy external connecting terminals **9'** are formed at corner portions of the board. In FIG. **11**, the external connecting terminals are formed at the center portions and corner portion of the board. In FIGS. **12** and **13**, the external connecting terminals are formed at the center portion of the board as blocks and at the corner portions of the board. In other words, the flat type external connecting terminals are formed with constant pitches in a lattice shape. However, depending on the number of external connecting terminals, the arrangement thereof can be freely selected. When the height of the rear surface of the board is kept constant, the reliability of the connections can be further improved. When the dummy external connecting terminals **9'** are formed at regions free from the external connecting terminals (these regions include at least corner portions), since the height of the rear surface of the board is kept constant, the external connecting terminals **9** can be equally contacted with the circuit board. As long as the flat type external connecting terminals are formed with constant pitches in a lattice shape, the semiconductor chip can be tested through a standard semiconductor socket. In other words, since the terminal pins are formed with constant pitches in a lattice shape and a standard semiconductor socket with terminal pins that have elasticity, the semiconductor package can be tested. The dummy external connecting terminals **9'** may be formed outside the lattice arrangement with constant pitches.
> (Emphasis added.)

Iwasaki '890 does not describe or suggest that these dummy connectors can be provided in "at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent

thereto", as recited in Claim 20. Accordingly, Claim 20 is independently patentable for at least these additional reasons.

Finally, Claim 14 also is independently patentable. Claim 17, the recitations of which have now been included in Claim 14, was rejected in view of the two Iwasaki references and U.S. Patent 5,796,169 to Dockerty et al. In addition to the recitation of signal conductors, Claim 14 also recites:

> ...wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array....

The Official Action notes at the bottom of Page 8, that Iwasaki '890 does not describe or suggest "at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array". In an attempt to supply the missing teaching, U.S. Patent 5,796,169 to Dockerty et al. has been cited, specifically noting the support solder **16** of Figure 3. However, this support solder is placed at corners of the array, as noted by Dockerty et al. Column 4, lines 35-50:

> FIG. 3 schematically depicts the ball grid array surface of integrated circuit device **3** according to the present invention, including some refinements thereof. Chevron like, L-shaped support elements, generally at **14**, are added to the corner regions of the integrated circuit device ball grid array surface. The support elements are preferably composed of high melting temperature solder, typically the 90/10 lead/tin composition, and extend from each corner along the axes of the ball grid array over multiple solder ball spacing increments. For example, support solder **16** extends over 4 solder spacing increments while support solder **17** extends over three increments. Support solder **18** only extends one solder ball increment in each axial direction while remaining symmetrically within the range of the pattern defined by support solder **16**. (Emphasis added.)

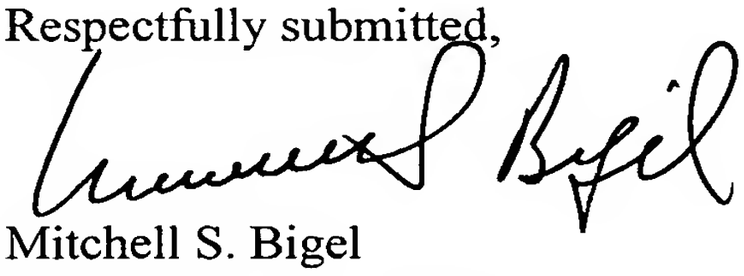
Accordingly, Dockerty et al. does not describe or suggest "at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto and electrically strapped together", as recited in the above-quoted recitations of Claim 14. Accordingly, Claim 14 is independently patentable for at least these additional reasons.

For at least these reasons, independent Claims 8, 14 and 20 are patentable over Iwasaki '890, Iwasaki '882 and/or Dockerty et al. The pending dependent claims are patentable at least per the patentability of the independent claims from which they depend.

Conclusion

In order to expedite allowance, many of the claims have been canceled, and the remaining independent claims have been amended. As was shown above, the cited references do not describe or suggest the recitations of the pending claims. Accordingly, Applicants respectfully request withdrawal of the outstanding rejections and allowance of the present application.

Respectfully submitted,



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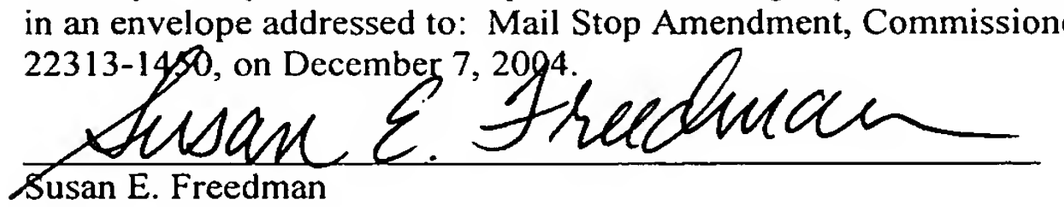

Susan E. Freedman
Date of Signature: December 7, 2004